**SRM Institute of Science and Technology**

Mode of Exam

**OFFLINE**

**SET B**

**College of Engineering and Technology**

**DEPARTMENT OF ECE**

SRM Nagar, Kattankulathur – 603203, Chengalpattu District, Tamilnadu

**Academic Year: 2021-2022 (EVEN)**

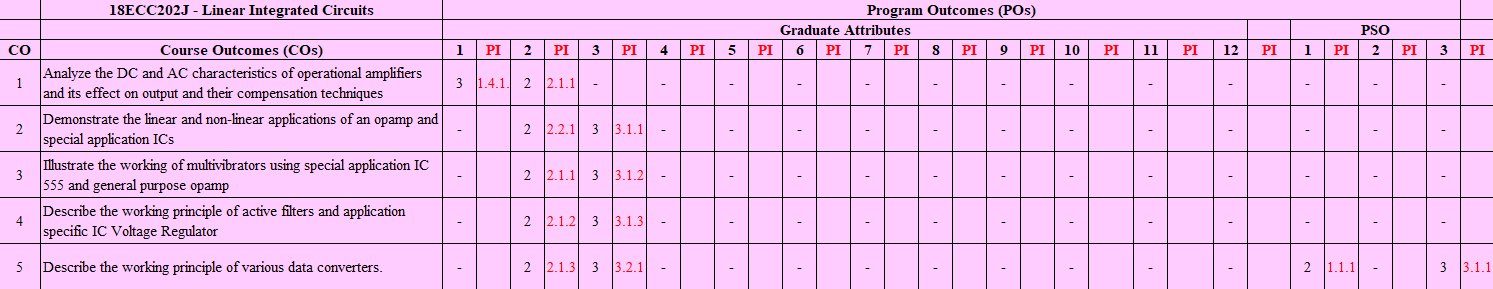
**Batch 2**

**Test: CLAT-3** **Date: 27/06/22**

**Course Code & Title:** 18ECC202J / Linear Integrated Circuits **Duration:** 2 Periods

**Year & Sem:** II year / IV Sem **Max. Marks:** 50

**Course Articulation Matrix:**

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| **Part - A**  **(10 x 1 = 10 Marks)**  **Instructions: Answer ALL** | | | | | | |
| **Q. No** | **Question** | **Marks** | **BL** | **CO** | **PO** | **PI** |
| **1** | The change in output voltage for the corresponding change in load current in a 7805 IC regulator is defined as   1. All of the mentioned 2. Line regulation 3. **Load regulation -Ans** 4. Input regulation | **1** | **1** | **2** | **2** | **2.2.1** |
| **2** | The 7812 regulator IC provides \_\_\_\_\_\_\_\_.  A. 5 V  B. -5 V  **C. 12 V-Ans**  D. -12 V | **1** | **1** | **2** | **2** | **2.2.1** |
| **3** | The frequency when the gain drops by 3 dB is  A. Band frequency  **B. Cut off frequency-Ans**  C. High frequency  D. Low frequency | **1** | **1** | **2** | **2** | **2.2.1** |
| **4** | The lower and upper cut off frequency of a band pass filter is 2.5khz and 10 khz. Determine the bandwidth   1. 750 Hz 2. **7500Hz-Ans** 3. 700Hz 4. 70Hz | **1** | **1** | **2** | **2** | **2.2.1** |
| **5** | How can a first order low pass filter can be converted into second order low pass filter  A. By adding LC network  **B. By adding RC network-Ans**  C. By adding RC || LC network  D. By adding RLC network | **1** | **1** | **2** | **2** | **2.2.1** |
| **6** | The number of comparators used in 5 bit flash ADC is  **A. 31-Ans**  B. 32  C. 4  D. 5 | **1** | **1** | **3** | **2** | **2.1.1** |
| **7** | A dual slope ADC uses 16 bit counter with analog voltage of 4.12V and VR=6V. Its binary equivalent is   1. 1010111111001001-Ans 2. 1011111111001001 3. 1010111101001001 4. 1010100111001001 | **1** | **1** | **3** | **2** | **2.1.1** |
| **8** | Flash type ADC requires \_\_\_\_\_ resistors for 4 bit conversion   1. 3 2. 15 3. 4 4. **16-Ans** | **1** | **1** | **3** | **2** | **2.1.1** |
| **9** | The maximum deviation between actual and ideal converter output after gain and offset errors have been removed is   1. Absolute accuracy 2. **Relative accuracy -Ans** 3. Relative /absolute accuracy 4. Linearity | **1** | **1** | **3** | **2** | **2.1.1** |
| **10** | Calculate the values of the full scale output for an 8-bit DAC for the 0 to 10 V range.  A. 9 V  B. 6.961 V  C. 10 V  **D. 9.961 V -Ans** | **1** | **3** | **3** | **2** | **2.1.1** |
| **Part – B**  **( 4 x 10 = 40 Marks)** | | | | | | |
| **SECTION B1**  **Instructions: Answer ANY 2 Questions** | | | | | |  |
| 11 | Derive the transfer function of a second order filter whose frequency response is shown below and find the expression for Damping coefficient.  LowPassFilter_T2        Diagram-2 marks,deivation -8marks | 10 | 3 | 2 | 3 | 3.1.1 |
| 12 | Draw the cicuit diagram of Twin -T Notch filter.Obtain the expression for bandwidth and quality factor  Notch filters use a twin-T parallel resistance-capacitance (RC) network to obtain a deep notch. Higher values of Q can be obtained by feeding back some of the output to the junction of the two tees.        **Diagram-3marks**  **Deivation -7marks** | 10 | 3 | 2 | 2 | 2.2.1 |
| 13 | Explain how the curent limit and curent fold back are achieved in IC723 voltage regulator curent limit      curentfoldback  **Diagram-2marks each ,Explanation-3 maks each** | 4 | 2 | 2 | 2 | 2.2.1 |

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| **SECTION B2**  **Instructions: Answer ANY 2 Questions** | | | | | | |
| 14 | i)Explain the working operation of Flash type ADC.  ii) What are its merits and demerits?  i) A 3-bit Flash ADC consists of seven comparators, a resistive voltage divider circuit that contains 8 series resistors, and a priority encoder. The input analog voltage is applied to the positive terminal of the comparator while the reference voltage is applied to the negative end of the comparator. Each comparator compares the input voltage to the reference voltage.  If the input voltage is lesser than the reference voltage of the comparator then the output of the comparator is low. Whereas if the input voltage is greater than the reference voltage of the particular comparator then its output will be high.  Flash ADC | Digital-Analog Conversion | Electronics Textbook  Explanation -3marks,diagram-3marks,derivation -2marks  ii) What are its merits and demerits?  **Merits**  It is the fastest ADC and is utilized in high bandwidth applications.  **Demerits**  These ADC are more power-consuming as compared to ADCs implemented with different techniques.  It is a limited resolution of up to 8-bits.  Increase bits lead to a large die area. With an 8-bit resolution, it needs a die area big enough to accommodate 255 comparators (2^N-1).  The resistors and comparators should be matched to provide an accurate reference voltage to the comparators by the voltage divider network.  **Marks-2** | 8  2 | 3 | 3 | 2 | 2.1.1 |
| 15 | i)Describe the operation of successive approximation type ADC .  A successive approximation ADC is a type of analog-to-digital converter that converts a continuous analog waveform into a discrete digital representation via a binary search through all possible quantization levels before finally converging upon a digital output for each conversion. The successive approximation Analog to digital converter circuit typically consists of four chief subcircuits:  1. A sample and hold circuit to acquire  the input voltage (Vin).  2. An analog voltage comparator that  compares Vin to the output of the  internal DAC and outputs the result of the comparison to the successive approximation register (SAR).  3. A successive approximation register subcircuit designed to supply an approximate digital code of Vin to the  internal DAC.  4. An internal reference DAC that, for comparison with V, supplies the comparator with an analog voltage equal  to the digital code output of the SARin.-----------**6marks**  ------**2marks**  ii)What are the advantages of dual slope ADC.  Advantages: It is more accurate ADC type among all. It has greater noise immunity compare to other ADC types.  Disadvantages: It is the slowest ADC among all. In order to achieve better accuracy, it requires high precision external components.  **Each 1 mark** | 8  2 | 3 | 3 | 2 | 2.1.1 |
| 16a | A dual slope ADC uses a 16-bit counter and a 4 MHz clock rate. The maximum input voltage is +10 V. The maximum integrator output voltage should be - 8 V when the counter has cycled through 2n counts. The capacitor used in the integrator is 0.1 µF. Find the value of the resistor R of the integrator.  **Solution**:  Time period (t2 – t1) = 216 / 4 MHz = 65536/ 4 MHz = 16.38 ms---**2m**  For the integrator  ∆𝑣0 = −1𝑅𝐶𝑉𝑎(𝑡2 − 𝑡1)  So, RC = -(10 V/ -8 V) 16.3 ms = 20.47 ms------**2m**  R = 20.47 ms / 0.1 µF = 204.7 kΩ = 205 k Ω-----**2m** | 6 | 4 | 3 | 2 | 2.1.1 |
| 16b | In the previous problem, If the analog signal Va is +4.129 V. Find the equivalent digital number.  **Solution**:  Since, Va = VR (N / 2n)  So the digital count N = 2n(Va/ VR)  = 65536 (4.129 V / 8 V) = 33825 --------------**2m**  for which the binary equivalent is 1000010000100001- **-- 2m.** | 4 | 2 | 3 | 2 | 2.1.1 |